Measured Loading Speed of Maxim's Serial Interface Software

This application article presents the three-wire bus speed generated by Maxim software running on various personal computers. Processor speeds tested ranged from 233MHz to 933MHz. Windows 95 and Windows 98 operating systems were used. The parallel printer port of the PC is monitored with a logic analyzer to capture the serial bus transmissions. The 24-bit register of the MAX2361 is loaded in 204µs to 118.4µs, depending on the operating system and the processor clock frequency.

Additional Information: Wireless Product Line Page
Quick View Data Sheet for the MAX2360
Applications Technical Support

Maxim provides software to program the internal registers of many products using the three-wire SPI (serial peripheral interface) bus. The software accomplishes the bus loading operation by "bit-banging"[1] on the parallel printer port of a personal computer. One undocumented aspect of this software is the speed at which the data is transported over the serial bus. Many SPI ICs support clock rates of 10MHz or greater. This application note presents the serial interface performance on a variety of computers. The load time for a 24-bit long register, such as found in the MAX2361, ranged from 118µs to 204µs on average. The software used for this test is the "Maxim Interface Software Version 5.00.26".

The Test Environment

Four different IBM compatible PCs were used to evaluate the impact of different processor clock speeds, memory sizes, and operating systems.

Table 1: Personal Computers Used to Test Software

	Dell 4100 Desktop	IBM T20 Notebook	HP Pavilion 6470Z Desktop	Sony Vaio PV220 Desktop

Operating System	Win 98 Second Edition	Win 98 Second Edition	Win 98	Win 95
Processor (P = Pentium)	P III	PIII	PII	PII
Processor Speed	933MHz	750MHz	400MHz	233MHz
DRAM	128M	96M	96M	32M

On each machine, only one parallel printer port is installed. To monitor the signals appearing on the printer port, a logic analyzer was connected as show in Figure 1.

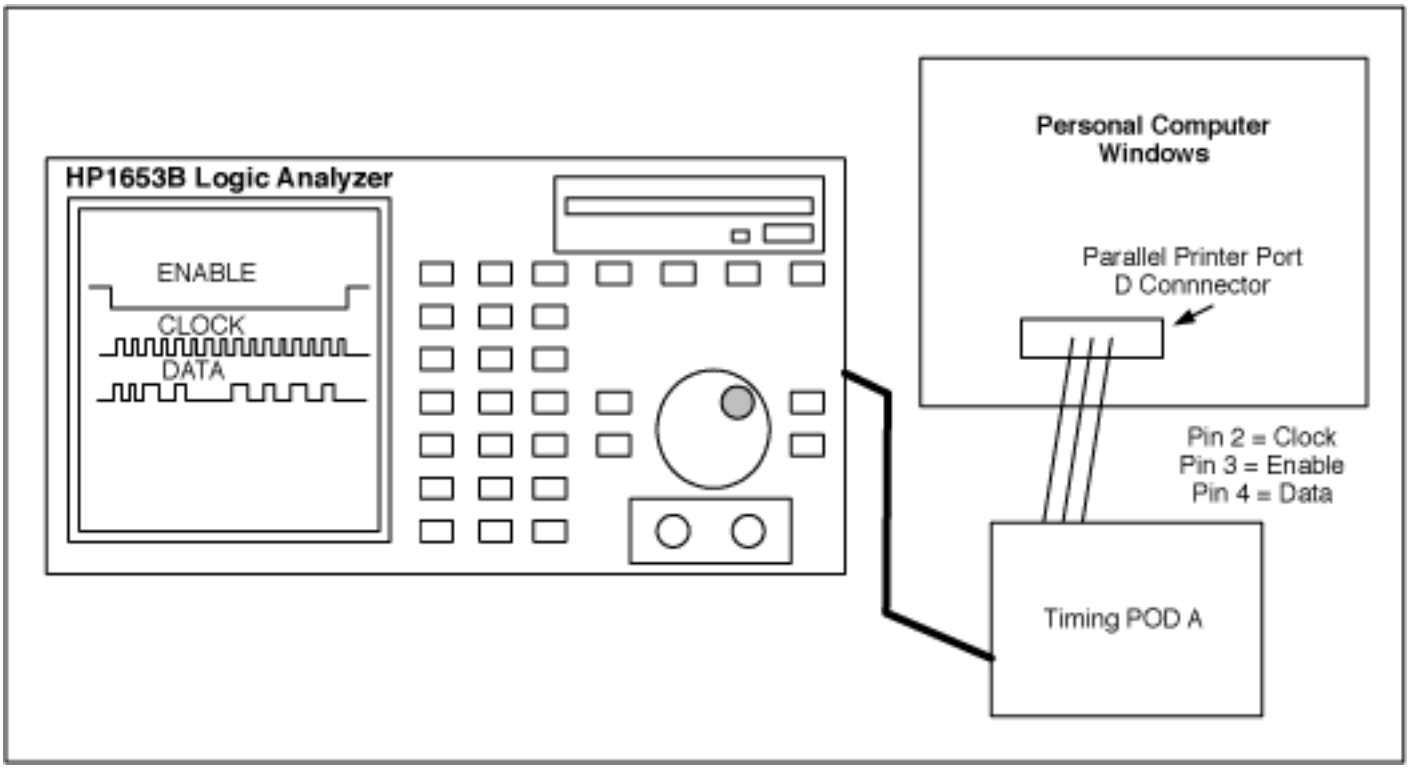

Figure 1. Interface between the logic analyzer and the personal computer

The Test Procedure

The interface software was loaded and executed on each machine. The MAX2360 "Register View" screen was used to cause the software to send out a 24-bit register value. The register chosen is the RF R Divider, with a default value of 1968. The binary pattern transmitted is 000000000111101100000001. The first seven bits of this register are not used, and the next 13 bits program the RF (radio frequency) reference divider of the phase lock loop to divide by 1968. The last four bits transmitted on the parallel printer port are the destination address of the value in the MAX2360/61. The value of 1968 is a typical one used in CDMA systems to divide the 19.68MHz VC-TCXO (voltage controlled temperature compensated crystal oscillator) down to 10kHz. This then sets the RF phase detector comparison frequency to 10kHz.

The logic analyzer used in the HP1653B. The three pins of the parallel printer port that need to be monitored when using the interface software with the MAX2361 are pins 2, 3 and 4. Pin 2 carries the SPI bus signal "Clock", Pin 3 carries SPI signal "Enable", and Pin 4 carries "Data". The logic analyzer was configured to trigger on the falling edge of the enable pulse. The total load-time is defined as the total time the enable signal is LOW. Figure 2 presents the screen capture from the HP1653B.

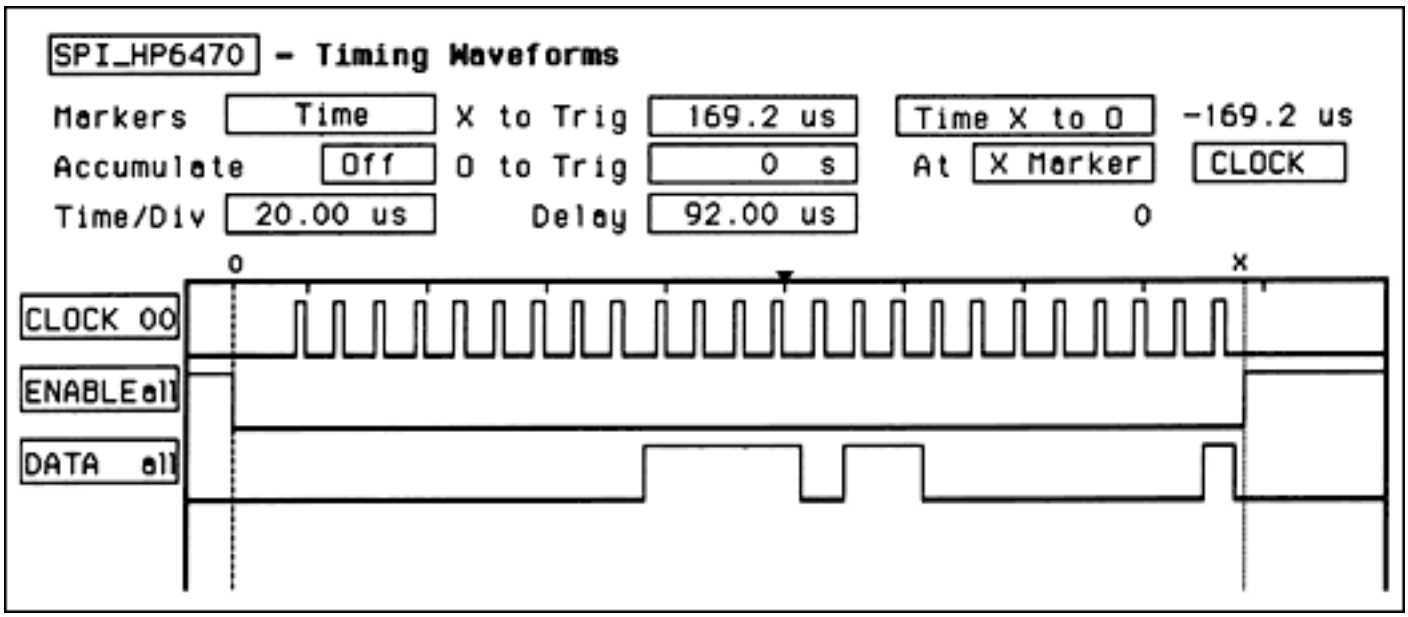

Figure 2. SPI bus transfer captured by HP1653B

Discussion: Interpreting Logic Analyzer Results

After studying many SPI bus transactions under control of the interface software, it becomes clear that some judgement is needed to state a simple numerical result. The speed of transfer is mainly influenced by two factors:

1) The processor clock speed. Fast processor speed supports fast SPI transfer.
2) The operating system overhead.

Windows will suspend processing of the application program at seemingly random times to service system overhead interrupts. Some transactions extended the SPI transfer interval by 30% to 50%. This did not happen frequently in the tests.

Historical Note: MS-DOS used a system timer interrupt that happened 18.2 times per second (about every 55ms, Interrupt 08_H). Windows 9X may have a similar timer resource that will interrupt the system and at those times the SPI bus activity is suspended until the interrupt is cleared.

Any abnormally long SPI transfer times were discarded. The purpose was to find the typical speed, not the slowest. The vast majority of captured transactions clustered tightly about a single value.

Results

The SPI transfer times ranged from 118µs to 204µs on average. In keeping with the "principle of minimum astonishment"[2], it was found that the fastest processors gave the fastest SPI transfer times. See Table 2 for the measured results.

Table 2: SPI Transfer Time on Different Personal Computers

	Dell 4100 (Maxim Machine)	IBM T20 Notebook	HP Pavilion 6470Z Desktop	Sony Vaio PV220 Desktop
Operating System	Win 98 Second Edition	Win 98 Second Edition	Win 98	Win 95
Processor (P = Pentium)	P III	PIII	PII	PII
Processor Speed	933MHz	750MHz	400MHz	233MHz
DRAM	128M	96M	96M	32M
2360 SPI Load Time	118.4µs	135µs	169µs	204µs

The results are presented in Figure 3 in graphical form. Also shown at the bottom of the graph is the speed at which many SPI ICs can accept serial data. With a 10MHz SPI clock, the 24-bit load operation should be completed in 2.5µs, which is 50 times faster than the bit-banging technique. This would seem to imply that the PC clock would need to run at greater than 46GHz! (This is a false conclusion, as the limiting factor is very likely the speed supported by the I/O bus of the PC, and not the processor clock.)

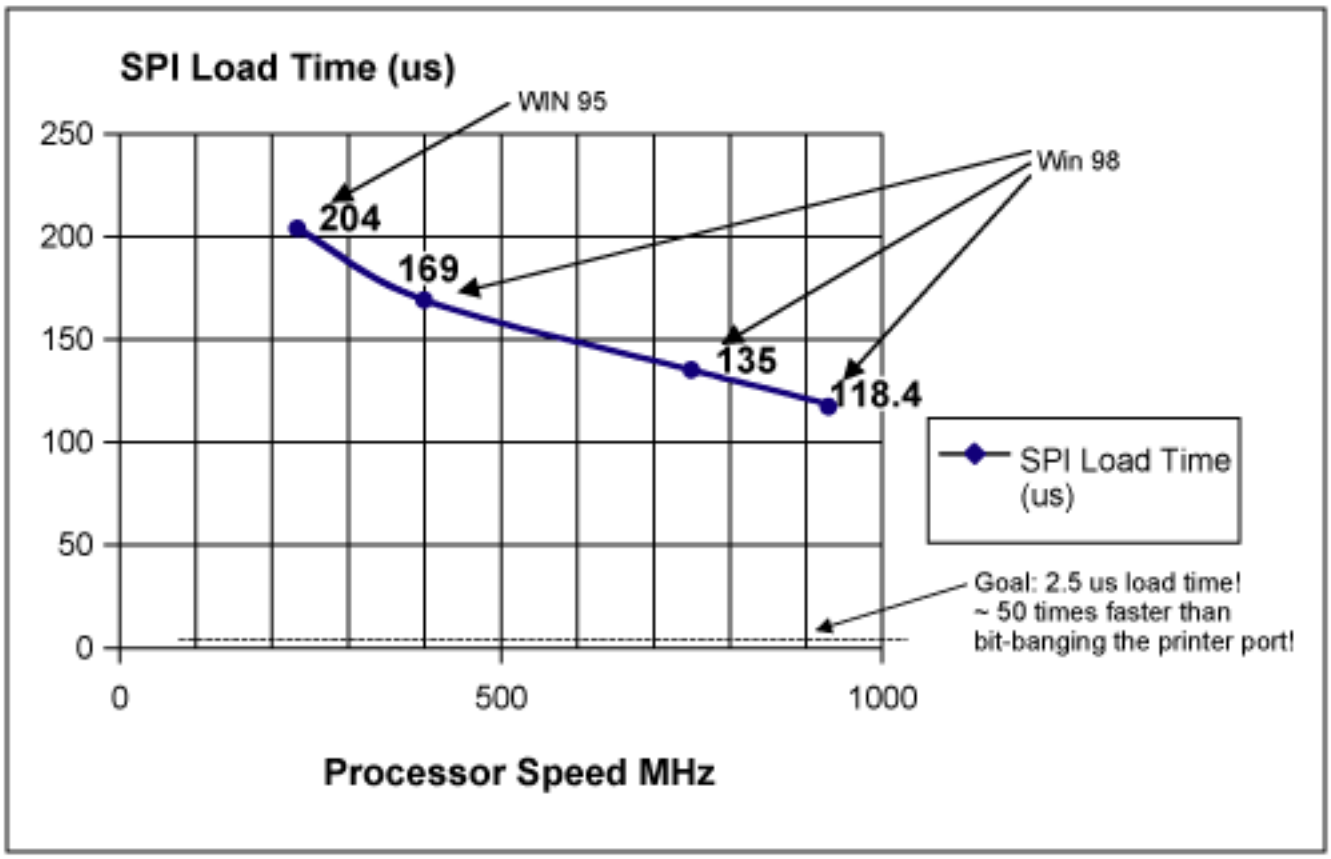

Figure 3. SPI transfer time decreases as the PC clock increases

References

IBM Personal Computer Hardware Reference Library; *Technical Reference 6025008* (First Edition August 1981) International Business Machines Corporation.

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1 Bit-banging describes a technique whereby pins on a microcontroller are forced high or low under direct software control. This technique, in the context of personal computers, usually refers to the software directly manipulating the pins of the parallel printer port.

2 Taub and Schilling: "*Principles of Communications Systems,*" page 249, McGraw-Hill Book Company, New York, 1971.

More Information

MAX2360:	QuickView	--	Full (PDF) Data Sheet	-- Free Samples
MAX2361:	QuickView	--		-- Free Samples